Forth computer

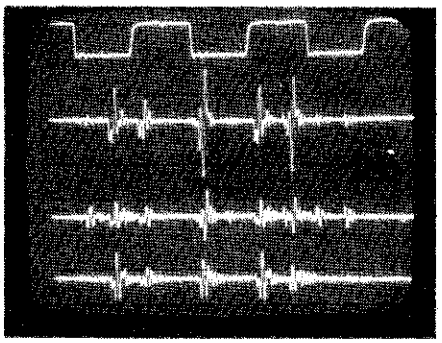
Construction tips for the 6809-based Forth computer – part four.

by B. Woodroffe

Most of the prototype version of this computer was constructed on one wire-wrap board. The number of signal buses rendered anything other than a multilayer printed circuit board an impractical solution without splitting the circuit into sections. Splitting the circuit was rejected to eliminate buffers associated with long cable runs. Wire wrapping provides connections at least as good as solder joints through cold welding between the wire and edges of the pin.

All main memory, refresh circuit, microprocessor rom and interface i.cs are mounted on the main 229 by 178mm board, as are the video-display processor and memory. The analogue video gate and RS232 driver are built on two 16-pin dip headers. User-port hardware and the disc-drive interface between the floppy-disc controller and the drive are housed on a second wire-wrap board. There are many connections on the board so a powered wrapping tool, a stripping tool and different coloured wires for different functions are useful. Copper-clad board was used for the power supply, which should be constructed before the main processor board.

Dynamic ram takes little static current but substantial pulses, reaching toward 80mA per device over a few nanoseconds on some clock edges. Although the rams work within a 10% voltage tolerance, for reliable operation substantial local decoupling must be included in the +12 and −5V rails to overcome power-line inductance; each ram has a 0.1μF ceramic capacitor on both supplies. Further 10μF bulk decoupling capacitors were used, one between each four devices. Decoupling capacitors for the 5V rail were used throughout the design at the rate of one 100nF component for each six i.cs. As with the RAS/CAS/WE damping resistors, the design seems robust since the ram was initially built and worked without decoupling (see photograph).



Voltage transients at the 4116 dynamic rams showing from top to bottom the E clock signal and +12V, +5V and −5V supply lines with a 200ns/div timebase.

This is a large project and all construction errors were found to be the result of either miswiring or plugging in the i.c.s wrongly. Dynamic rams I currently use got very hot when I plugged them in back-to-front. Construction should start with a minimum system, i.e. c.p.u., p.i.a., eproms and a 16K ram. At switch on, the lamp connected to the p.i.a. B-port D_0 line will go on then off. The state of this lamp then monitors the state of i/o data on the line. Ram-select lamps will stay off. V.d.u. hardware is self-contained so an idea of its performance can be seen on a tv screen without involving the main processor as the video i.c. generates its own characters.

Connection of the parity circuit to HALT should only be made after the ram circuits are known to work, i.e. when the system ready message can be displayed consistently. Should the RS232 connection fail to work, the most likely cause, especially if a signal at the a.c.i.a. output can be seen on resetting, is that data lines on pins two and three are crossed. Another problem could be that the RS232 terminal

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Main-board components

Resistors

Value	Qty	Function
10k	8	pull-up, FIRQ, IRQ, NMI, VFOE, RESET, video and RS232 output
10k	2	pull-out parity, video ram, 9-resistor sil packs
100	1	dot-clock
500	1	dot-clock trimmer
20k	1	monostable timing, 5%
400	4	pull-up, led
33	5	damping, RAS, CAS, R/W
75	1	video output
150	1	video output
1k	5	video and RS232 output
2.3k	1	video output
4.7k	1	video output
2k	1	video output
2k	1	video output, trimmer
5.1k	2	RS232 output

Capacitors

Value	Qty	Function
100μ	2	+5V decoupling, 25V
20μ	2	+12V decoupling and reset, 25V
10μ	8	−5V and +12V decoupling, 25V
100n	57	−5, +5 and +12V decoupling
20p	2	crystal decoupling, 10%
51p	1	dot clock, 5%
20p	1	monostable timing, 5%

Integrated circuits

Ref	Qty	Pins	Type	Comments
11	1	14	LS280	parity checker
12-110	9	16	4116	see note
21	1	28	I3242	address multiplexer
22-210	9	16	4116	see note
31,67	2	20	LS245	bi-directional buffer
32-310	9	16	4116	see note
41,44	2	14	LS04	hex inverter
42,47	2	14	LS00	quad 2-input NAND
43,72	2	12	LS02	quad 2-input NOR
45	1	16	LS112	dual JK bistable multivibrator
46,53	2	16	LS161	sync. binary counter
47,48	2	14	LS37	quad 2-input NAND clock driver
51	1	40	M6809A	microprocessor, 1.5MHz
52	1	16	LS139	dual 2-to-4 decoder
53	1	14	LS122	monostable multivibrator
54	1	40	WD1793	floppy-disc drive controller
55	1	40	M6821	p.i.a.
62,63	2	24	I2732	4K by eprom, T_{acc}=450ns
56	1	16	LS175	quad D bistable
66	1	16	LS157	quad 2-to-1 line multiplexer
71	1	24	M6850	a.c.i.a.
73	1	14	LS86	quad 2-input ex-OR gate
74	1	14	LS132	quad 2-input Nand, schmitt
75	1	28	EF96364	video display controller
76	1	20	LS240	octal 3-state inverter
77,78	2	18	2114	1K by 4 static ram
81	1	14	LS00	quad 2-input NAND
83	1	14	LS04	quad 2-input NOR
84	1	16	LS161	sync. binary counter
85	1	24	I2716	2K by 8 eprom, T_{acc}=450ns
86	1	20	LS273	octal D bistable
95	1	16	LS165	8-bit serial shift reg.

See note for other i.c. locations

Other components

2N2222	5	video, RS232 output transistors
1N4150	2	video, RS232 output diodes
2N2907	1	RS232 output transistor
L.e.ds	4	parity checking, high-efficiency red

6.00MHz crystal
1.008MHz crystal
DIP headers for video and RS232 output
25-pin D-type connector for RS232 output
Single-pole two-way switch for display-page select
Three, 16-way insulation-displacement connectors
Vero 07-0130A wire-wrap board
Wire-wrap pins (1 packet), wire, tool, un-wrap tool and wire stripper. **Wire-wrap sockets:**

Pins	Quantity
14	14
16	39
18	4
20	4
24	4
28	2
40	3

Notes

Memory circuit was designed using Mostek MK4116-3 data sheet and most critical timing specification was T_{acc} = 135ns (column-address strobe). Positions $IC_{57,82,92}$ are 16-pin dil for plugs a,b and c respectively. Positions $IC_{91,93}$ are also 16-pin dil for RS232 and video signals. Resistors are 10% and capacitors are +80/−20% except where tolerances are given.

Disc interface

Type	Qty	Pins	Comments
LS244	1	20	octal buffer
*38	2	14	standard t.t.l. quad NAND, o.c.
LS123	1	16	dual monostable multivibrator
LS161	1	16	4-bit binary counter
LS163	1	16	4-bit binary counter
LS74	1	14	dual D bistable multivibrator
LS14	1	14	hex inverter, schmitt
LS04	1	14	hex inverter
K1160	1	14	8MHz oscillator (Motorola)
LS138	2	16	3-to-8 line decoder

Power supply

MC3405	op-amp/comparator, alternative 158 op-amp and 193 comparator
LM7812	12V, 1A regulator
2N2222	n-p-n (4 off)
2N2907	p-n-p (2 off)
2N4036	p-n-p (2 off)
2N6476	p-n-p (2 off)
2N4443	s.c.r.
1N437	ref. diode, alternative 1N960B 9V zener
1N4371	zener, 2.7V
1N4372	zener, 3V, alternative 2.7V
1N751	zener, 5.1V
1N963	zener, 12V
MR852	fast recovery diode
MDA970-2	bridge rectifier, 4A
1N4150	diode, alternative 30V switching diode, pref. Schottky
HLMP-1300	high-efficiency red led, 2.2V drop

Capacitors

1n	10%
470n	(2 off)
100n	(2 off)
22µ	10V tantalum
22µ	20V
1m	12V low equivalent series resistance, e.g. Sprague 672D046 or Dubilier UPC1052
8m	40V, alternatively 4m

Resistors

0.13	1W
100	(2 off)
133	0.25W
200	
680	0.25W
1k	0.25W (6 off)
1.5k	
1.96k	
3.16k	(2 off)
10k	(6 off)
28.7k	
75k	
100k	(5 off)
50k	preset pot.

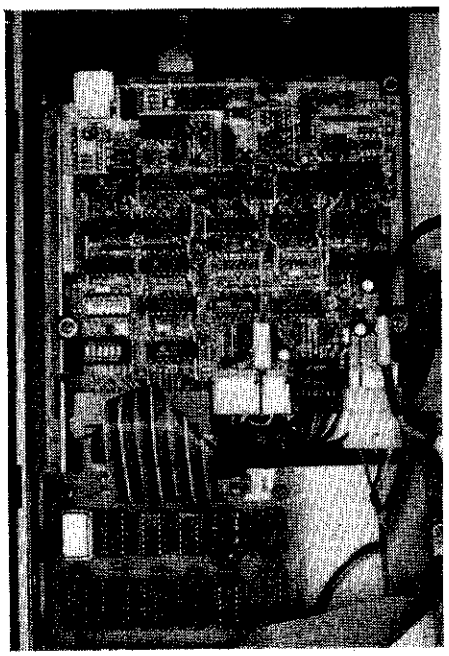
Transformer is a 15V r.m.s. 2A type and should be protected by a 500mA slow fuse. A mounting kit is required for the 2N6476, a cooling tab for the T05 transistor, and the toroid is an Arnold A-930157-2 with 35 turns of 21 s.w.g. (not 19 s.w.g. as on the drawing). The toroid is available from Walmore Electronics Ltd, 11 Betterton Street, Drury Lane, London WC2H 9BS.

Other components

Wire-wrap socket, 14 pin (4 off)
Wire-wrap socket, 16 pin (10 off)
Wire-wrap socket, 20 pin
Wire-wrap board 176 by 110mm, e.g. Vero 02-0120H
34-way insulation-displacement connector
34-way insulation-displacement cable to drive
Disc drive, e.g. Teac FD50A (up to 4)
Drive power connector (AMP1-480424-0)
Pins for above connector (AMP60617-1, 60619-1, 4 off)
Decoupling capacitors, 100n (6 off)
Decoupling capacitor, 100µ
Input resistors, 333 (4 off)
Input resistors, 220 (4 off)
Timing resistors, 30k (2 off)
Timing capacitor, 2µ 10V
Timing capacitor, 33µ 10V

Alternative oscillator components

Hex inverter, LS04
Resistor, 464 (2 off)
Capacitor, 20p
Crystal, 8MHz



Wire-wrapped disc interface board bottom, and the disc-drive main circuit board.

takes too much current from the −5V supply, an indication being that the rams persistently give parity errors on power up which disappear when the RS232 terminal is disconnected. Forth response OK is preceded by the stack depth.

The problem of driving capacitive loads with l.s.t.t.l. outputs showed up as undershoot in signals passing from the interface board to the controller. Although the prototype worked with the undershoot, it was cured by taking an inverted version of the required signal back to the main board and inverting it there with a spare l.s.t.t.l. gate. Capacitance of the insulation-displacement connection between the two boards was avoided in this way. Spare connections on the inter-board connector should be grounded and ground should be placed near active signals, e.g. clocks, disc data.

Although for 8K of memory one gets a compiler and operating system and programming and execution unit there is still much to be done. I think that games are one of the best ways to learn about computers for the definition of a problem to be solved is often as difficult as solving the problem. Forth is particularly suited to games programs — the *Byte* game contest was won by a game written in Forth[10].

Reference

10. A. Saunton-Angus, Cosmic conquest, *Byte*, Dec. 1982, p.124.

Further reading

C. H. Ting, Systems Guide to Fig-Forth, Mountain View Press.
Forth Dimensions, Forth Interest Group, PO Box 1105, San Carlos, CA94070 (house magazine for members).

Brian Woodroffe has found a way of speeding up disc operations and data-transfer rates so that faster units such as the Sony Microdrive and 8in drives can be used with the Forth computer. Descriptions will follow.