Forth computer

Interface circuits and software for disc-drive control are main subjects of Brian Woodroffe's third article describing his 6809-based microcomputer. First, operation of the video controller is concluded and i/o software discussed.

by Brian Woodroffe

Character-code and row information for the video-controller i.c. is supplied as an address to a character rom. Character information for each row is fed to an LS165 shift register and serial output from this register is combined with synchronization signals in an analogue gate to give a standard 1V p-p composite-video signal which is subsequently fed to a u.h.f. modulator.

The dot clock, consisting of a Schmitt-trigger relaxation oscillator, should be adjusted to the minimum frequency to minimize the luminance bandwidth required in the monitor consistent with all text displayed on the screen. Character values 10 to 1F hexadecimal are programmed into the character rom to give coarse graphics. Two 2114 rams hold enough information for one 1024-character Forth screen to be displayed.

Two further video rams store text normally lost at the top of the screen. A switch allows a page of lost text to be displayed.

Terminal and i/o software

The Forth reset routine checks to see if there is an M6850 present and if not automatically redirects terminal i/o routines from the RS232 interface to the p.i.a. for parallel i/o. Forth words giving access to user ports are included in this operating system. These words, P@and P! act in the same way as Forth words @ and ! except that they allow access to user i/o ports.

The software-driven output word, P!, makes data available on the p.i.a. B lines then activates the address coded on the A lines. On-input, P@, reads data while the port address is made. Output ports ideally connect to LS273 latches and input ports to LS244 buffers. Port-strobe lines are decoded from the p.i.a. A lines using LS138 three-to-eight-line decoders. Eight read and eight write ports can be connected to this hardware and if more ports are needed then a further 6821 p.i.a. could be connected and mapped into the USER variable-address area. Cursor control codes, i.e. decimal codes for EMIT, are as follows.

8 left (backspace)
9 right (tab)
10 down (line feed)
11 up
12 home and erase
13 carriage return
14 home
15 carriage return and line erase

Disc interface hardware

Interfacing to the floppy disc[6] is done using the most readily available controller since it is cheaper than using s.s.i./m.s.i. devices. Complexity of the WD1793 controller is comparable to that of the 6809. The first problem was interfacing an 8080 style peripheral to the M6809 bus, the main difficulty being the writing data-hold times.

The problem of data-hold times was solved using the memory-ready signal, MRDY, which when active (low) holds the processor clock cycles in an E-not-Q state for at least one quarter of a bus cycle. This quarter cycle provides the hold time. The memory-ready signal triggers a monostable multivibrator each time the procesor wants access to peripheral-drive address space between C000 and DFFF on the rising edge of the Q clock and this signal forms the floppy-disc controller write signal.

A read signal is derived from clocks E and Q. Interrupt and data-request outputs of the floppy-disc controller are connected to the processor FIRQ pin so that data transfer can take place using the M6809 SYNC instruction. As noted before, a floppy-disc drive's data rate can cause problems when d.m.a. is not used. In double-density recording on a 5¼in floppy using a WD1793 controller, the worst-case data-transfer rate is 27μs/byte. Coding is shown in Table 1.

The trick is that SYNC stops the M6809's execution without affecting the clocks until the floppy-disc controller interrupt occurs and the processor resumes execution. This provides quick synchronization between the processor and controller. Despite that modifying the direct-page register gives quicker access to the f.d.c. which is in high memory, this feature was not used because of the extra coding needed. Had the processor clock been slower this alternative might have been necessary.

Interfacing the floppy-disc controller to the drive is the next problem. Most of this is covered in an ANSI standard[7] but the problem of clock recovery remains. Because of mechanical constraints, data read from disc will not be synchronous with any processor clock so clock information contained in the data stream must be extracted. In single-density recordings each bit cell has a clock bit and a possible data bit (no data bit is zero) and in double-density recording the position of the bit within the cell determines whether it is a one or a zero. A clock synchronous with incoming data is required to determine the incoming bit's position.

Although it gives the best performance, a phase-locked loop circuit was rejected on grounds of cost. Instead a crystal clock running at eight times the nominal read clock is used and a divide-by-eight version of this clock is phased with the incoming data to recover the original clock. First the incoming bit stream is synchronized to the crystal clock (×8) to produce pulses with accurately defined widths using an LS74. This pulse stream is fed to the floppy-disc controller (RAW READ).

The reading clock is provided by an LS161 counter which is normally held off until the controller wants to read the disc, when the counter is enabled by the read-gate signal. This counter would normally free run at about the nominal clock rate, but it is synchronized by applying the raw read signal to its load input. The load frequency locks its D output (READ CLOCK) so that it changes mid-way between input bits. As the maximum number of bit cells without read bits is three, the recovered clock never gets too far out of phase.

Table 1. Code showing how the M6809 SYNC instruction is used for floppy-disc drive data transfer.

	STB FDC	F7C000		send command byte to f.d.c.
BRED2	SYNC	13	2	wait for f.d.c. response
	LDB FDC	F6C000	5	get status
	BITB #2	C502	2	test byte-in
	BEQ BRERR	2710	3	no, then error
	LDA FDC+3	B6C003	4	get byte
	STA 0, Y+	A7A0	7	store, advance pointer
	LEAX −1,X	301F	5	reduce count
	BNE BRED2	26EF	3	loop back
BRED3	LDB FDC	D600		wait till
	BITB #1	C501		f.d.c. finishes
	BNE BRED3	26FA		
BRERR	RTS	39		

32 cycles at 1.5MHz = 22μs
Upon entry B=command code
Y=pointer to data destination
X=byte counter

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Problems with phasing are most noticeable when double-density recording is used, so a means of preventing bunching of the bits is used. Precompensation[8] prevents bunching by moving the written data bits slightly relative to the nominal position in a bit cell so that when the data is read back the bits appear to be in their correct positions. The matter of precompensation depends on the drive used. For those drives that do not require precompensation, including the TEAC FD50A used in the original design, the precompensation circuit is omitted.

The disc should be set to respond to its address and head-load on drive select and not to the motor-on signal, i.e. the TEAC FD50 disc drive should be set as follows (for further drives, follow the same pattern).

DRIVE 0
HS=set, MX=set, DS0 set,
DS1,DS2,DS3=unset,
HM=disconnected.
DRIVE 1 (if fitted)
HS=set, MX=set, DS1=set,
DS0,DS2,DS3=unset,
HM=disconnected.

Disc-interface software

Under command of the c.p.u., the floppy-disc controller takes care of head positioning, sector positioning, data serialization and cyclic-redundancy checking. As soft sectoring is used, sector positioning is determined by the address record read from the formatted disc. The controller may be programmed to format the disc. So long as certain inter-record gap and record sizes are adhered to, the formatted disc capacity may be increased, Table 2.

Different systems use different sector formats[9], numbers and sizes of sectors and sector numbering systems. In this system, all variables associated with disc formatting are defined by the user which means that most disc formats may be read. The sector size is written into the address record of each sector so it is possible for the system to adjust its buffer size to that of the disc. Forth word ?DISC is included to read the current disc and set parameters termed DENSITY, B/BUF and SEC/TRK to those associated with the disc. Only formats mentioned in Table 3 apply to the disc format program and ?DISC.

When formatting a disc, it can be advantageous to interleave the sectors on a track. With this in mind a dummy word SKEW was included which is currently defined as no operation, but it may be redefined to perform an interleaving algorithm during formatting, Table 3. Defining Forth word FORMAT for disc formatting is shown in Table 4.

Forth treats all disc memory systems in the same way, i.e. as a contiguous set of 1024byte screens, hence the choice of a v.d.u. Main Forth words used to gain access to screens on a disc are R/W, which moves data between a disc and memory, and BLOCK. As disc sector size depends on format, words BLOCK and constants B/BUF, bytes-per-sector, SEC/TRK, sectors-per-track, TRK/SIDE, tracks-per-

Table 2. Capacity of a formatted disc may be increased provided that certain record sizes and gaps are not exceeded.

Density	Single		Double	
Bytes/sector	128	256	256	512
Sectors/track	16	10	16	10
Bytes/track	2048	2560	4096	5120
Bytes/disc	82K	102K	160K	205K
Relative	100%	125%	200%	250%

side and SIDE/DISC provide a means for Forth to work out which sectors make up a screen. The size of virtual memory buffers in Forth should be the same size as a sector.

Time taken for the head to position itself over the relevant track is a major constraint when using disc drives. Other time factors for a 5¼in floppy-disc drive are motor start-up time, head-load time and rotational latency. To speed up access time for double-sided discs it is usual to physically combine two tracks on opposite sides of the disc into one logical track. This minimizes head seek time for it is likely that the sector required will be on the same bigger logical track and the time taken to gain access to the other side of the disc is governed by the time taken for an electrical switch to act rather than by the delay of a mechanical head seek. But since Forth treats all discs in the same way, including this feature would have meant that one could not mix single and double-sided discs.

When using the Teac FD50A disc drive, access time is dominated by the start-up time of 1s. If faster disc drives are used, time constants may be changed (discussed in a following article). Start-up time and head-stepping rate constants are moved into ram from eprom by the Forth start-up word COLD and may be modified to suit faster drives. Forth constants normally hold the values of constants in the parameter-field address (p.f.a.) but as this system is rom based, modification of the constants would not be possible so they are coded with a new routine which stores the value in ram. This list shows how the constant DENSITY is altered from single to double density and gives other constants and their meanings.

DENSITY =1 (double density, 0 for single density)
B/BUF =512 (number of bytes per disc sector)
SEC/TRK =16 (number of sectors per disc track)
TRK/SIDE= (number of tracks on disc, normally 35-40 for a mini-floppy)
SIDE/DISC=1 (2 for double-sided)
SEC-OFST =1 (for numbering sectors 1 to n, 0 for numbering 0 to n−1)

1 (value to store, returned after execution of DENSITY)
' DENSITY (find DENSITY p.f.a. address)
@ (p.f.a. in this special constant points to constant position)
! (store 1 there)

Power supply

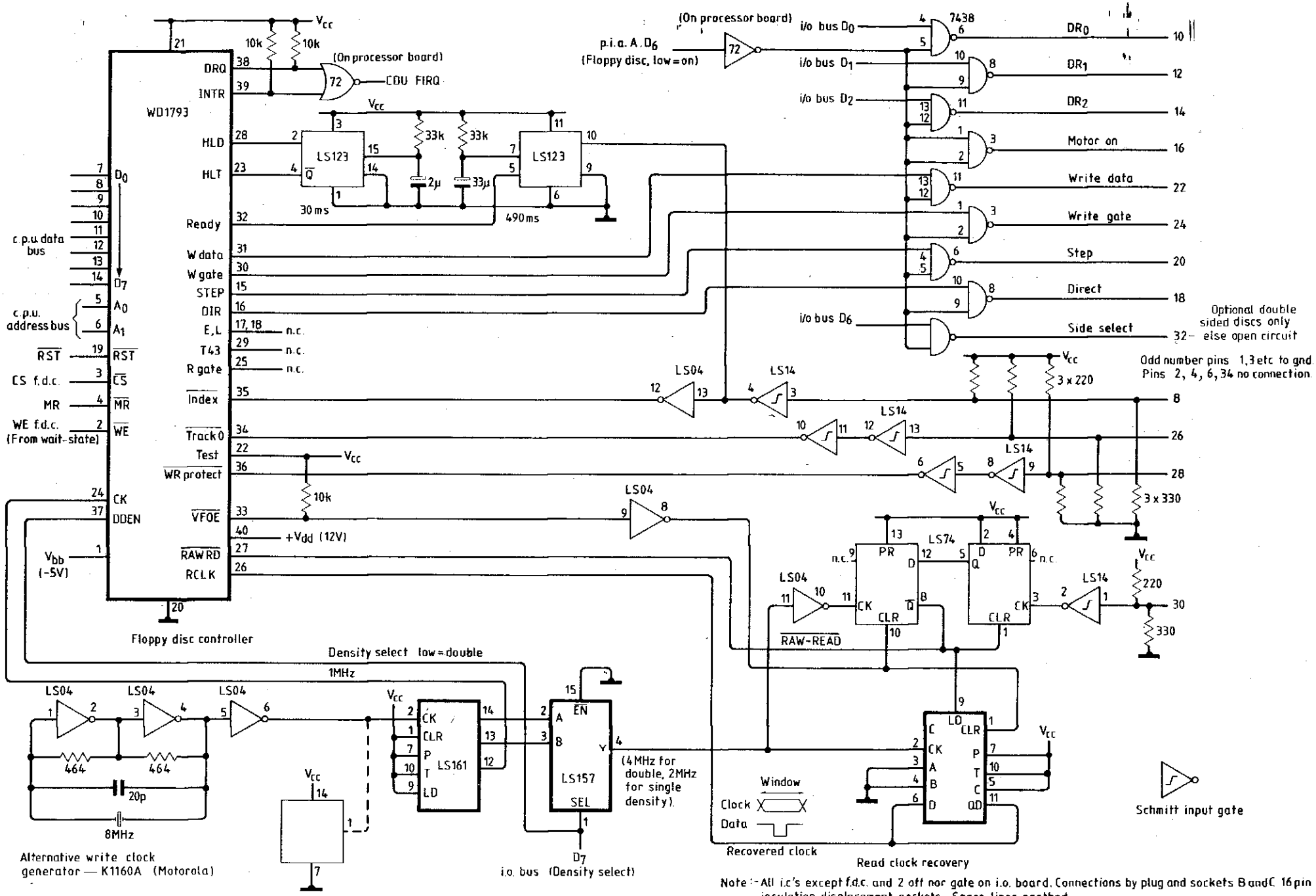
Only one 15V secondary winding is required on the transformer to provide a low-current −5V supply for biasing the dynamic rams, +12V for the rams and floppy-disc drive and +5V for all logic circuits. A minimum value for the unregulated supply is determined by the 12V rail; unregulated input should be 20V to ensure adequate regulation with low mains supplies. Heaviest current demands are on the 5V supply and using a linear regulator to provide this rail would have resulted in excessive heat generation with a loss of efficiency so a switching regulator was designed.

Table 3. Example of a routine for defining dummy word SKEW to give interleaved formatting.

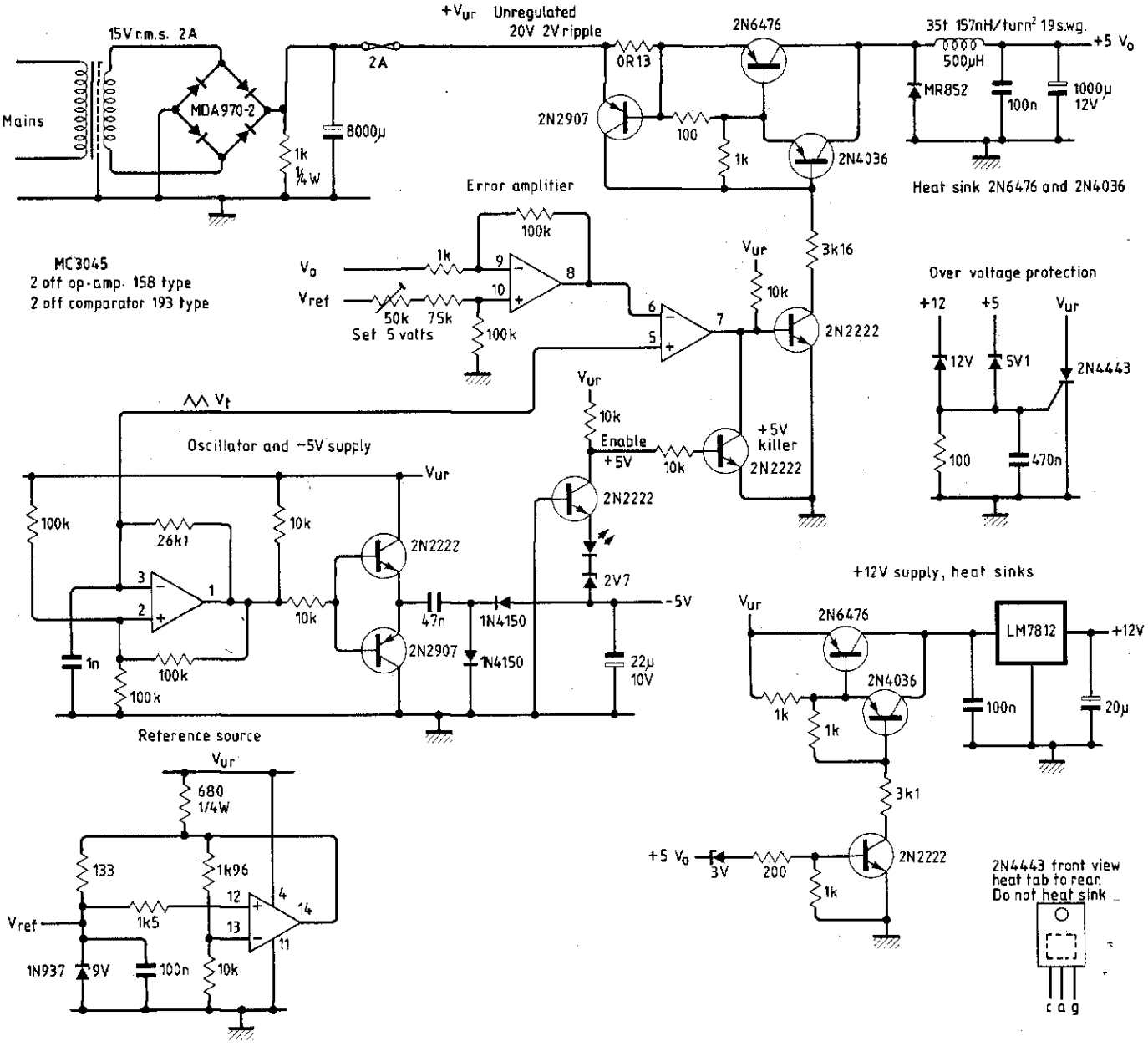
```
FORTH HEX                ( select Forth and hexadecimal number base)
: SKEW1 DUP              ( new word, duplicate sector # to be interleaved)
  1 AND IF               ( only even sectors are interleaved)
    SEC/TRK 2 / FE AND   ( sector offset by half the disc)
    + SEC/TRK MOD        ( add offset and keep with 0 . . . n−1 sectors on
                           track)
  THEN ;
' SKEW1 2 −              ( find c.f.a. of new interleaving address)
' SKEW !                 ( find old skew p.f.a. and overwrite no-op there)
```

Table 4. Routine for defining Forth word FORMAT for disc formatting.

```
: FORMAT                 ( start compiling the word format)
  0 DR-SEL 100MS RATE CMND   ( turn disc drive on, seek track 0)
  #SIDES 0 DO            ( do for both sides)
    TRK/DISC 0 DO        ( do for all tracks)
      DP @               ( save pointer to scratch area)
      I J BLD-TRK WR-TRK ( build up image of track, write it out)
      ." track/side/status=" I . J . . CR   ( inform user, 0=good status)
      1 STEP             ( step in for next track)
      DP !               ( recover scratch area)
    LOOP
  RATE CMND LOOP         ( for other side)
  DE-SEL ;               ( turn drive off, finish compilation)
FORMAT                   ( carry out format)
```



Note :- All i.c's except f.d.c. and 2 off nor gate on i.o. board. Connections by plug and sockets B and C 16 pin insulation displacement sockets. Spare lines earthed.
Side select is open circuit when double-sided disc drives are not used



Switch-mode power supply uses one 15V r.m.s. secondary winding for +12V, −5V and high-current +5V rails. Frequency of the relaxation oscillator is 17kHz, giving the best compromise between smoothing component sizes and loss in efficiency due to switch transition times eating away at the duty cycle. Gating ensures that dynamic rams receive their three supply rails in the correct sequence and s.c.rs provide overvoltage protection.

After bridge rectification and capacitive filtering, the 15V r.m.s. transformer output gives approximately 20V. Dynamic rams are sensitive to the sequence in which power is applied to them so the supply had to be designed so that −5V appears first, followed by +5V then +12V.

Heart of the switch-mode power supply is a relaxation oscillator, the squarewave output of which feeds a charge pump to produce about −20V peak. This is regulated by a zener diode to produce −5V. Reference for the +5V supply is a 10V zener diode connected in a feedback loop to maintain constant current even when the 20V unregulated supply varies. An error signal derived from the +10V reference and +5V supply, and the relaxation oscillator triangle wave are fed to a comparator. A portion of the triangle wave depending on the magnitude of the error signal is fed to the switching transistor. This pulse-width modulated base drive is disabled when the −5V supply is not present.

The free-wheel diode, inductor and smoothing capacitor are fed by the switching transistor and are chosen with the operating frequency in mind. Around 17kHz is used since it is the best compromise between high-frequency losses and component size. At low frequencies the smoothing capacitor and choke become too large and at high frequencies the switching transition time takes up a large portion of the cycle time and efficiency is reduced.

Unregulated supply passes to the 12V monolithic regulator under control of a transistor switched by the +5V supply. To prevent overvoltage problems, an s.c.r. is included which switches on and blows the secondary winding fuse if either the +5 or +12 rails rise too high.

To be continued with construction tips, parts list and vocabulary.

Disc interface uses a readily available controller which works out cheaper than an equivalent circuit using s.s.i./m.s.i. devices. Clock information in data read from disc is synchronized using a crystal-controlled oscillator running at eight times the rate of the incoming-data clock. The prototype computer has a standard Teac 51/4in floppy-disc drive.

References

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