Microcomputer design — 3

Practical realisation of a microcomputer system

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The previous two articles developed the theme of a microcomputer system in the order of microprocessor, memory, input/output and a practical example. This third article uses the term "microcomputer system" to mean a microcomputer (as defined in the November issue) acting together with a specific software package. When designing microcomputers, the most important features of the hardware are the trade-offs between prices and performance balancing hardware and software.

THIS ARTICLE begins to describe the practical realisation of a microcomputer system using principles outlined in the first two articles in this series. Referring to Fig. 4 of Part 1 (November issue) all components shown there are present in one form or another. Fig. 1 shows a version of that Fig. 4 which more nearly approximates to the kit hardware to be described. We shall deal first with input/output, then, in a later article, with memory and lastly the microprocessor itself.

The design aim for the hardware was to include as many features as possible for programme development while keeping the total cost of the components to a minimum. This aim was approached by designing from the peripherals inwards towards the central processor; and the peripherals chosen were: keyboard, serial i/o device and visual display, with a 16-line i/o as an optional extra. The price of the kit depends on the cost of the hardware, but this can be minimised by increasing the software, so it would seem that the software should be maximised. There is a feature of software which has to be borne in mind, and that is that e.p.r.o.ms (see November issue) occur in units of 1024 bytes. Again for cost reasons the maximum software allowed was fixed at 1024 bytes; in other words the software could be contained in a single MK2708 e.p.r.o.m. device.

*Shelton Instruments Ltd, the designers of the NASCOM I microcomputer kit (see November issue, p.45).

Peripheral 1 — the keyboard

The keyboard was reduced to its simplest form and is shown diagrammatically in Fig. 2. The circuit diagram is in Fig. 3. It is arranged as a single-port peripheral and the port address has been chosen as zero (P_0 in Fig. 1). The hardware realisation includes two integrated circuits to obtain latched outputs and gated inputs; thus 16 lines are available for port zero, eight in and eight out. Further use has been made of the output lines by choosing a 6-bit latch and using only

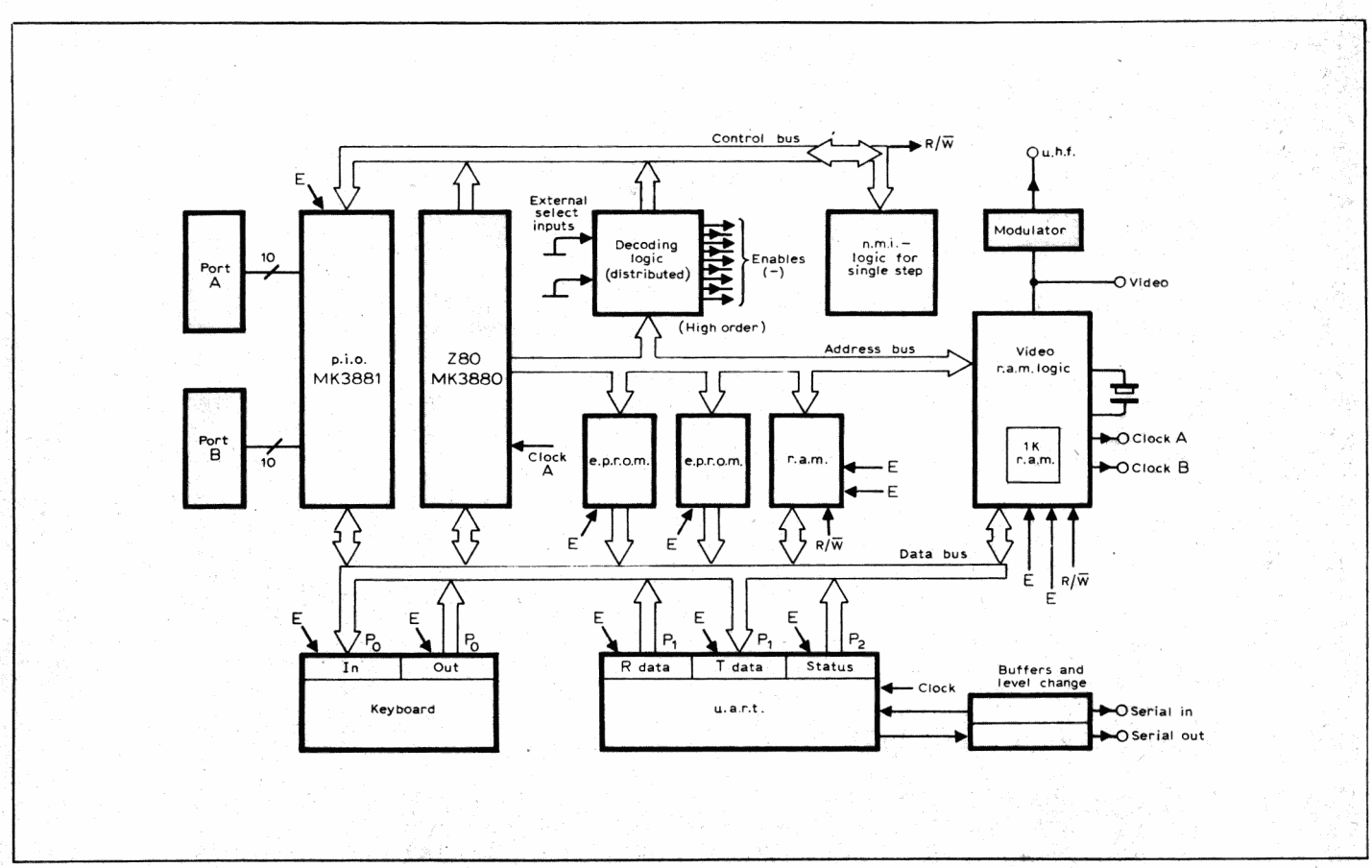


Fig. 1. *Block diagram of the microcomputer system. This can be related to Fig. 4 in the November issue and Figs 1 and 2 in the December issue. Part of the system is described this month, the rest in a later article.*

two of the lines for the keyboard. These two lines drive the clock and reset inputs of a counter decoder integrated circuit whose outputs are connected to columns of keys. To avoid phantom key appearances, a diode is connected in series with each contact. The matrix of keys is completed by six row lines, each driving a BC238 transistor amplifier which is connected to an integrated circuit forming the port input transmission gate. Output commands to port zero cause the data bus to be latched in an integrated circuit while input commands cause the keyboard row lines to drive the data bus.

Thus the c.p.u. has the opportunity to determine which keys on the keyboard are pressed, and it is left to the software to determine contact bounce elimination, change of state and code assignment.

There are one or two other features of note concerning port zero. The i.c. forming the port input transmission gate is an 8-bit buffer so that two bits are available to the user and do not interfere with normal keyboard operation. On the output side, the other bits of port zero from the second i.c. are used as follows:

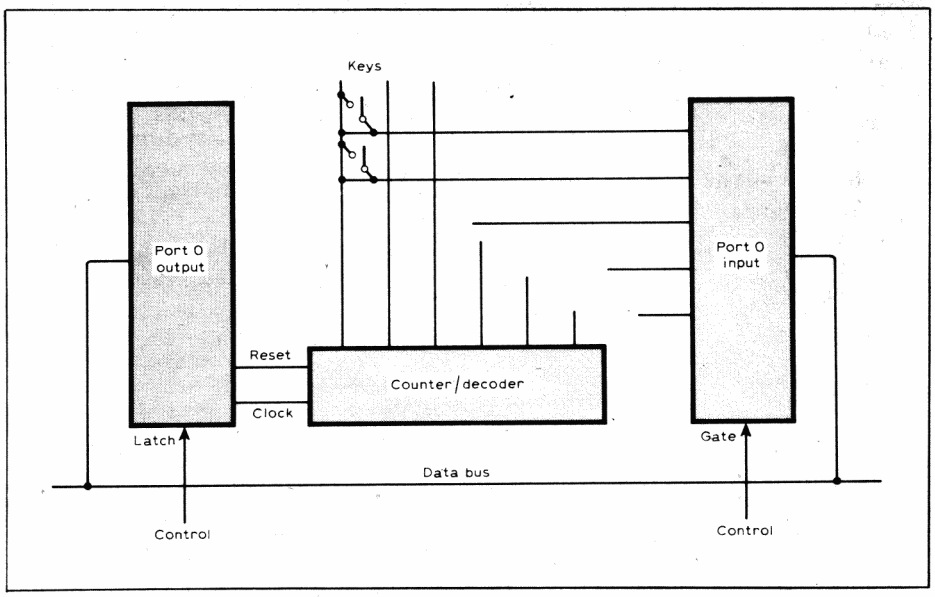


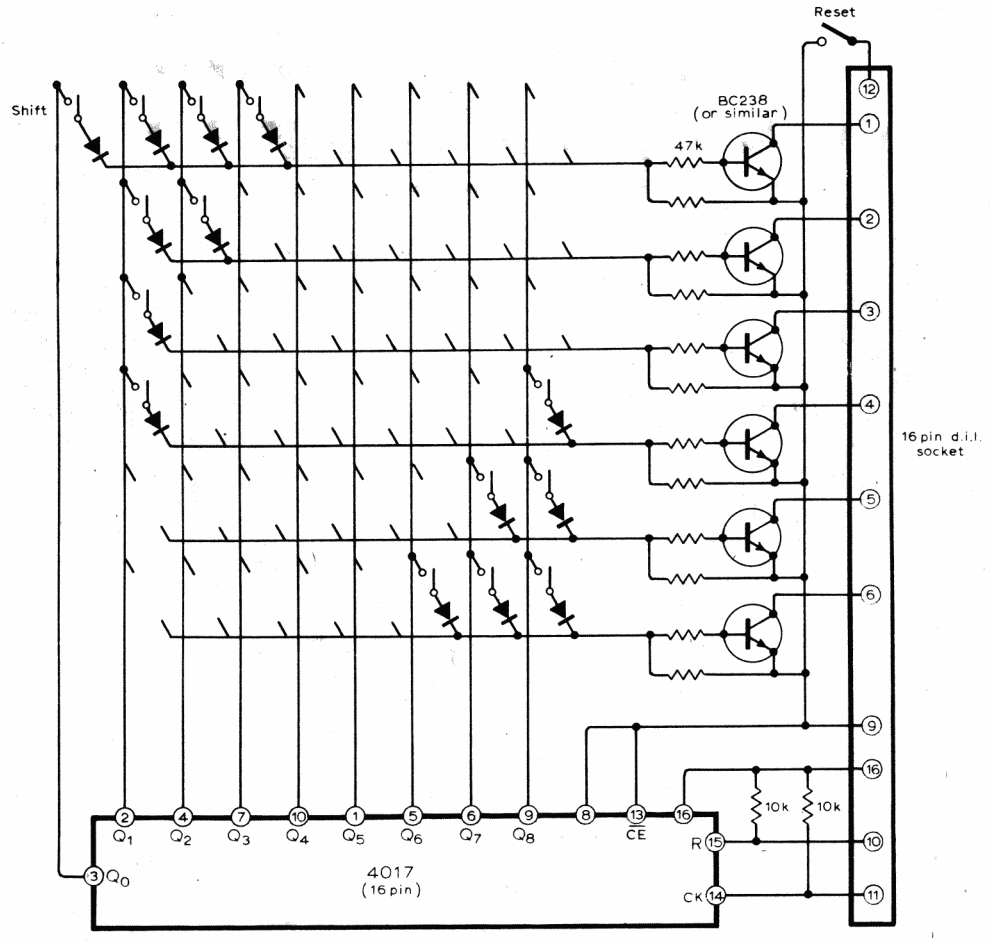
Fig. 2. *Simplified diagram showing essentials of the keyboard system.*

Q_2: available to user

Q_3: a low to high transition on Q_3 initiates a hardware single-step logic system to be described later.

Q_4: when Q_4 is high a transistor is energised to drive a light emitting diode. The software uses this to indicate that the

Fig. 3. *Circuit diagram of the keyboard and associated electronics.*



user should turn on the tape cassette drive. This can be modified to drive a relay to perform the drive start automatically.

Q_5: available to user.

Peripheral 2 — the serial i/o device

Since the data in the computing system is organised in 8-bit parallel form, some method of converting this to serial form on a single wire circuit is extremely useful. The basic requirement is a method for shifting a byte "sideways" into the single wire circuit. Such an operation appears the same from the outside whether performed by shift instructions or by means of a hardware shift register. The availability of suitable shift registers at very low cost and the limitation of software space combined to decide us to use hardware for the parallel to serial conversion. The device chosen is known as universal asynchronous receiver-transmitter (u.a.r.t.). It consists essentially of two shift registers, one to transmit and the other to receive; thus transmission and reception can take place simultaneously. To the processor the device is made to appear as two ports P_1 and P_2 (see Fig. 1). Data for transmission is fed to port 1. Similarly, received data is made available by taking it from port 1. Port 2 has no output significance but an input command causes "u.a.r.t. status" to be transferred to the data bus. The main signals of the status word are:

(1) bit 7 signifies that data has been received and can be obtained from port 1.

(2) bit 6 signifies that the transmitter is free to be loaded with data on port 1.

Other bits are connected to the data bus to indicate faulty reception if needed by the software.

Details of the u.a.r.t. circuits will be given in the next article, but the following remarks may be helpful at this stage. The rate at which data is shifted is determined by applying a clock signal to the receiver and transmitter clock inputs. The source of this clock signal can be one of three generators. There is a divider chain operating from a crystal oscillator elsewhere in the system, and a 5kHz clock signal is taken from this chain for operating the u.a.r.t. at 312.5 bits per second. Since a stop bit and a start bit are added to the byte there are 10 bits in each word transmitted. (By applying +5V to a pin on the device this can be increased to 11 bits by adding another stop bit.) Note that the baud rate is 8 × 31.25 whereas the bit rate is 312.5 bit/s. Since a baud is a bit/s of information, the start and stop bits should not be included. Thus the transmission rate is 31.25 bytes per second using this clock. The second clock source is a simple oscillator using the 555 integrated circuit which can be adjusted to operate at 1760Hz, and this, when two stop bits are sent, puts the data in a format suitable for use with teleprinters. The third clock source is simply any external clock the user may care to apply.

Serial data signal conditioning

There are basically two types of external device which will be connected to the serial i/o system. These are audio cassette recorders on the one hand and conventional teleprinters or v.d.us or serial data inputs to other computers on the other. For cassette recorders, a modulated tone is required. This is obtained by gating the 5kHz clock signal with the serial data, and the result can be attenuated if necessary by the user to suit his audio cassette recorder. The playback signal from such a recorder is a series of tone bursts corresponding to the serial data stream. A tone detector circuit is made up from an integrated circuit and associated components to recover conventional logic levels from the tone signal. The serial input to the u.a.r.t. may not be derived from two sources and so the input must be linked to the data source chosen by the user. Conventional serial devices use one of two conventions for data transmission, either RS232 or 20mA current loop. Both these are provided by discrete components and can be taken via a socket. The output is available in all three forms, RS232, 20mA loop and tone, simultaneously but the input may occur on only one.

Peripheral 3 — parallel i/o

The parallel input/output (p.i.o. in Fig. 1) is an l.s.i. package, type MK3881 from the Z80 set of microcomputer components. The p.i.o. has its registers' addresses defined by hardware selection logic but its function is programmable. The device interfaces the Z80 c.p.u. to the user's circuits by providing 16 lines, which may be either input or output, together with additional "handshake" signals. The p.i.o. has interrupt logic to deviate programme execution on a change of external logic state if required □

Part 4 of this series will describe the remainder of the microcomputer system. The microcomputer kit, NASCOM I, is available from Lynx Electronics (London) Ltd., 92 Broad Street, Chesham, Bucks (tel: Chesham (02405) 75154).

Microcomputer show

Wireless World is one of the sponsors of Microsystems '78, a seminar and exhibition on microcomputers and other small digital systems to be held at the West Central Hotel, London, February 8, 9 and 10. Information from Chris Hipwell, Room 125, Dorset House, Stamford Street, London SE1 9LU. See also advertisements.

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superimposed. This extra information can be obtained from the fuse manufacturer. With large and expensive installations it is also necessary to take into account the effects of overload, either cyclic of non-repetitive, and the possibility of heavy currents from capacitors.

For small equipment such as radio receivers and amplifiers, miniature fuses are used. A most popular type for many years was the 1¼ × ¼in to BS:2950. These can be obtained with current ratings from 50mA up to 25A. The corresponding voltage rating is reduced from 1000V. for the lowest currents to 32V at the highest currents. The fuses are colour coded and are available in quick blowing types with a maximum voltage of 250V. Recently, the 20 × 5.2mm fuse to BS:4265 and IEC 127 has been more extensively used with current ratings from 32mA to 6.3A. With miniature quick acting fuses the element is a very fine wire and tends to have relatively high arc voltages on operation. This depends on the resistance and reactance in the circuit and the instant when the fault occurs. A number of tests made on 200mA fuses with random point-of-wave switching on a 240V circuit showed that in one case a peak arcing voltage of 350V occurred. A diode in this circuit would therefore require a maximum repetitive peak reverse voltage of 400V.

Fuses to BS:4265 can be obtained with a wide range of operating speeds which are marked on the fuse link; FF is very quick acting, F is quick acting, M is medium time lag, T is time lag, and TT is long time lag. Various methods are used to meet the range of speeds, including the use of different materials such as silver, copper, nickel-chrome alloy or the use of two metals. Anti-surge fuses are available which withstand surges of $10I_n$ for up to 20ms. In this type the element often consists of two parts, one of which is a small spring soldered to a thin wire. Eutectic solder may be used to connect the element to the end cap and a low melting point alloy may be used for the junction.

The M effect, first described by Metacalf, is often used with medium time lag fuses. In a very precise machine operation, a small blob of solder about 2½ times the diameter of the element wire is placed on the element. The melting point of the alloy is very much lower than the wire and results in a longer operating time and a lower fusing factor.

Acknowledgement. The author wishes to thank Mr. P. G. Newbery of Brush Fusegear Limited for his assistance. □