A scientific computer — 2

Memory, v.d.u., tape and teleprinter interface

by J. H. Adams, M.Sc.

THE STANDARD COMPUTER holds up to 8 kilobytes of memory, but this can be expanded up to 32 kilobytes if necessary. Of this memory, 3K are 2708 r.o.ms which are mapped, or located, at the hexadecimal addresses 0000 to 0BFF. The first 2708 contains a monitor program using hexadecimal data, and responds to commands entered in English. The remaining two r.o.ms hold the more complex BURP monitor and interpreter.

Addresses 0C00 to 1FFF accommodate up to 5K of 21L02 read/write memory and these i.cs are grouped in eights, each one being the store for one bit in an 8-bit byte as shown in Fig. 6. The computer will operate with only 2K of r/w.m., these being IC_{22} and IC_{26}, but, for greater program storage, further blocks starting with IC_{23} should be added. Pin 12 of IC_{17} should be wired to pin 13 of IC_{22} and the position for IC_{21} left blank. This has been provided for any future development which may require more r.o.m. space.

The data outputs of IC_{18} to IC_{26} are wired to an eight-line bus which feeds into the main data bus through the tri-state buffer IC_{27}. Parallel wiring of the outputs is possible because the memory devices also have tri-state outputs. The chip-enable, CE, inputs are enabled by the outputs of a 3 to 8-line decoder, IC_{17}, which is, itself, only selected when $\overline{MREQ}$ and address line 15 are low, i.e. the Z80 must be requesting a memory operation in the lower half of the memory. Similarly, IC_{27} is only enabled when both $\overline{MREQ}$ and $\overline{RD}$ are low, i.e. a memory read is requested. A link has been placed in the $\overline{MREQ}$ line so that the system may be expanded as shown in Fig. 7. The $\overline{MREQ}$ is connected to a 74LS139 2 to 4-line decoder which is fed by A_{13}, A_{14} and the original MREQ. This modification generates four new $\overline{MREQ}$ signals, one for each quarter of a 32K memory. If the expanded memory is used, $\overline{MREQ}_1$ will take the place of $\overline{MREQ}$ on the original board.

As there are many devices to be

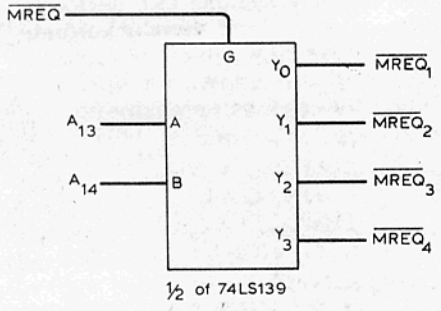
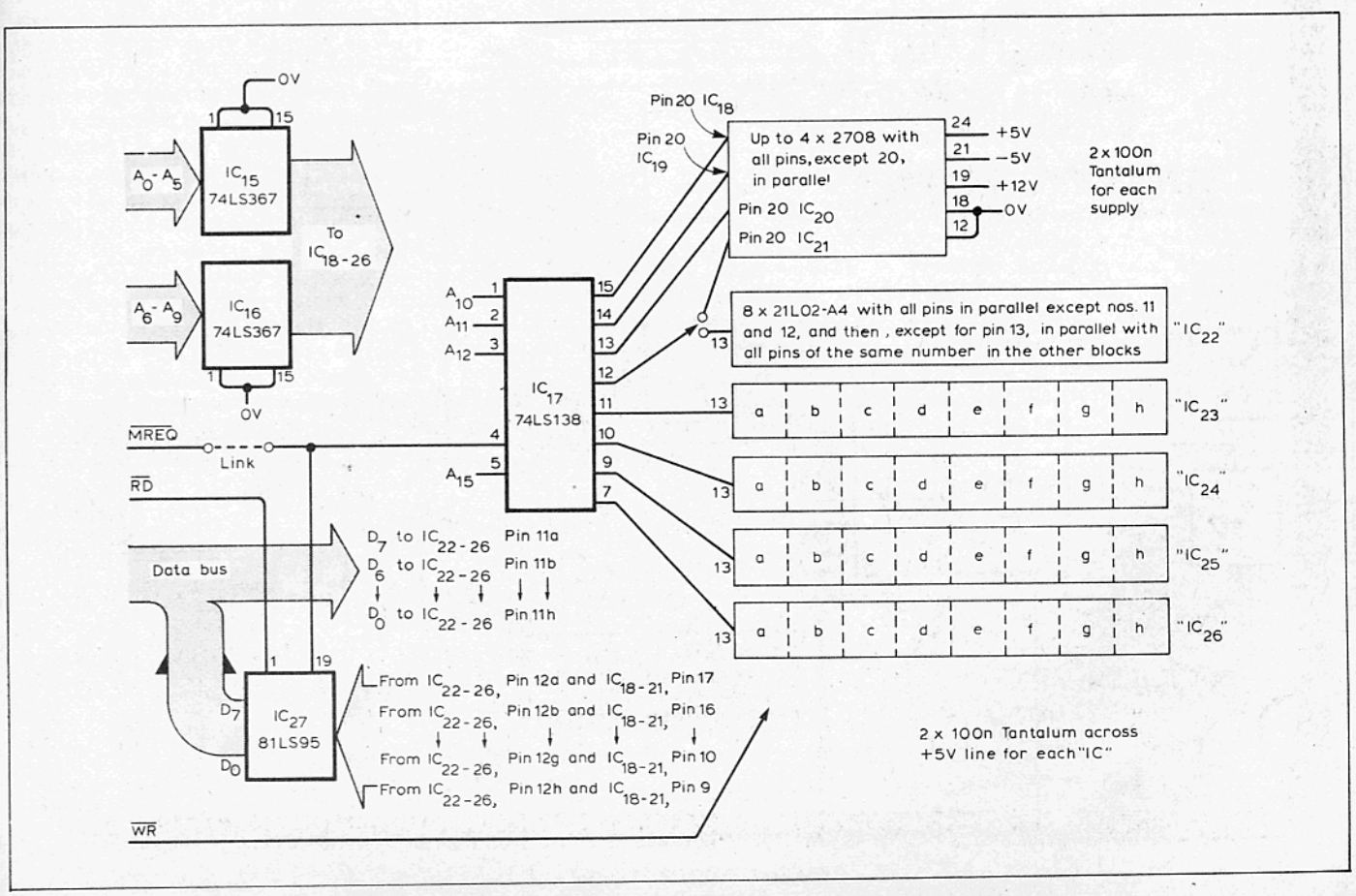


Fig. 7. *Modification to achieve four $\overline{MREQ}$ lines for the control of up to 32K of memory.*

Fig. 6. *Memory circuit. 3K of r.o.m. contains the monitor program, BURP monitor, and interpreter. 5K of r.a.m. accommodates user program storage. The memory can be extended in blocks of 8K up to 32K.*



driven from A_0 to A_9, these lines are buffered by IC_{15} and IC_{16}, which are permanently enabled. Although adding buffering increases the time delay between a memory request, and the data being ready for the Z80 to read in, the most critical 'reads' have 750ns to access the memory, therefore 21L02s with a 450ns access time are quite adequate.

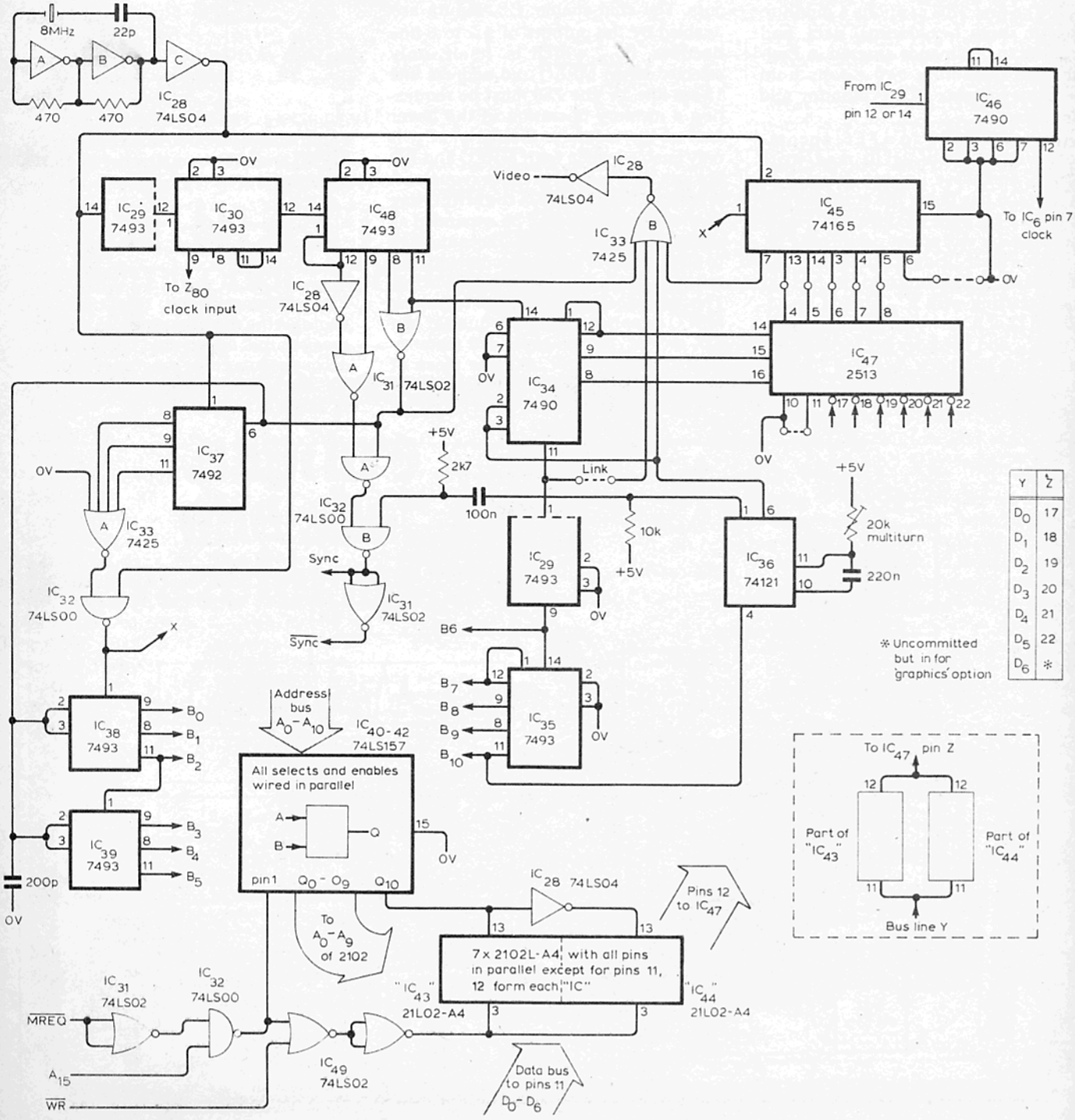
Visual display

The visual display circuitry in Fig. 8 is constructed using standard t.t.l. i.cs instead of one of the recent l.s.i. controllers. This approach was chosen because the only suitable l.s.i. device is rather expensive, and, more important, the t.t.l. design gives maximum flexibility and allows an optional graphics system to be easily implemented.

Each line scan takes 64μs and is thus compatible with standard 625 signals and, with 320 instead of 312.5 lines per picture frame, the frame scan, although slightly longer, will easily be within the range of a television set to be used as a v.d.u.

In Fig. 8., IC_{28} generates a signal at 8MHz from which all of the clocks within the computer are obtained. Part of IC_{29} divides the clock to 4MHz, and either the input or output of this i.c. is fed to IC_{46} which produces a true square wave at either 800 or 400kHz for the MM57109. The 4MHz is further divided by IC_{30} to provide a 2MHz clock for the Z80, and an output at 250kHz for IC_{48}, which produces 16 states of 4μs each. State 0001 is decoded and used as the line synchronizing pulse. The output at pin 11 of this i.c. is at 15.625kHz, and clocks IC_{34} at the standard 625-line rate. Part of the line sync. decoder, IC_{31b}, provides a signal which is active low during states 0100 to 1111 inclusive. This produces a 48μs burst during which IC_{33} and IC_{37} to IC_{39} are enabled, and allows a video display to occur, see Fig. 9. Division of the 64μs line scan into a 4μs sync. pulse, an 8μs pause, a 48μs display, and then a 4μs pause, allows for the overscan that occurs in commercial televisions. If the displayed video runs off the end of the screen, even with the width and shift controls adjusted correctly, omitting the inverter on pin 12 of IC_{48} will shift the displayed video 4μs to the left which corresponds to about five characters.

Fig. 8. *Visual display circuitry. This discrete t.t.l. version reduces cost and improves flexibility.*



The dividers described so far are free-running with their reset inputs taken low. The decade counter IC_{34} is fed with pulses at the line frequency and divides these to provide 10 row addresses for each line of displayed characters. Outputs Q_1 to Q_3 go directly to the character generator, IC_{47}, but Q_4 is connected to IC_{33} and is high during the ninth and tenth lines, i.e. the two lines to be blanked between character rows. A divide-by-32 counter, formed by IC_{29} and IC_{35}, provides an address for each line of characters on the screen. At the end of a display page, monostable IC_{36} is triggered by this counter to provide a reset pulse for IC_{34}. This holds the divider chain, IC_{34} to IC_{39}, at the first row of the first character of the first character row until frame flyback has occurred and line sync. has been regained. The monostable pulse is also used to blank the video during the flyback via IC_{33}, and through a differentiator, to provide a field synchronising pulse to IC_{32}.

A third divider chain remains reset except during the 48μs display time defined by IC_{48} and its associated gates. IC_{37} is clocked at 8MHz, and divides-by-6 to provide a character-rate pulse, which, when gated with the 8MHz clock, is used to load data from the character generator into the shift register IC_{45}. This gated pulse is also used to clock a character counter divide by 64 circuit, comprising IC_{38} and IC_{39}. Data loaded into IC_{46} comprises five bits of the row of the character which the character generator is being asked to supply, together with one blank bit on pin 6 to complete the 10 × 6 character format. These bits are loaded in parallel and clocked out serially, via pin 7, to the video gate, IC_{33}. The three lower address bits for the character generator, IC_{47}, are supplied by IC_{34} as previously explained. The upper six come from the r/w.m. comprising IC_{43} and IC_{44}. Addresses for this block of r/w.m. are supplied by the 2 to 1-line multiplexers IC_{40} to IC_{42}, which are switched between addresses supplied by the main address bus of the Z80 and those being generated by the v.d.u. dividers by the decoded $\overline{MREQ}$, $\overline{WR}$ and A_{15} signals. Because this signal also switches the R/$\overline{W}$ inputs of the memory, the conditions are either; multiplexer connects Z80 address bus to r/w.m., Z80 writes into r/w.m., or multiplexer connects v.d.u. circuitry to r/w.m., data inputs to r/w.m. disabled.

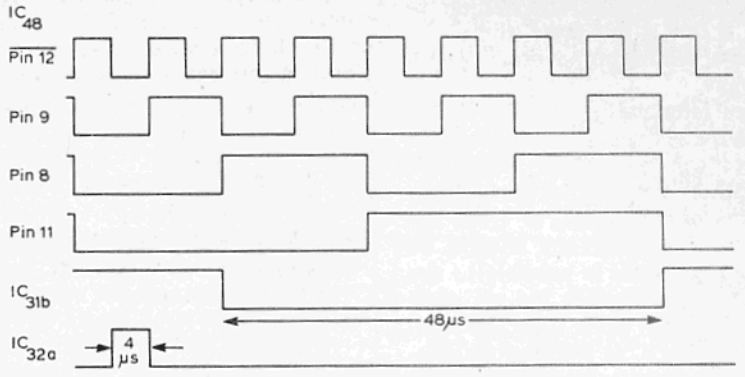


Fig. 9. *Divisions of the 64μs line scan.*

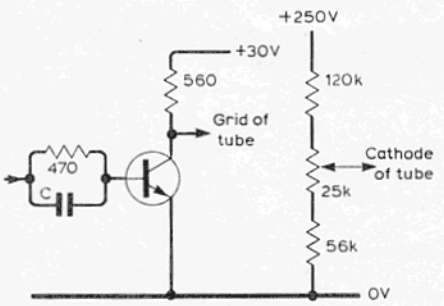


Fig. 10. *Typical television interface.*

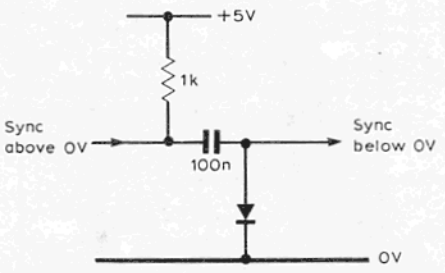


Fig. 11. *Positive to negative sync. converter.*

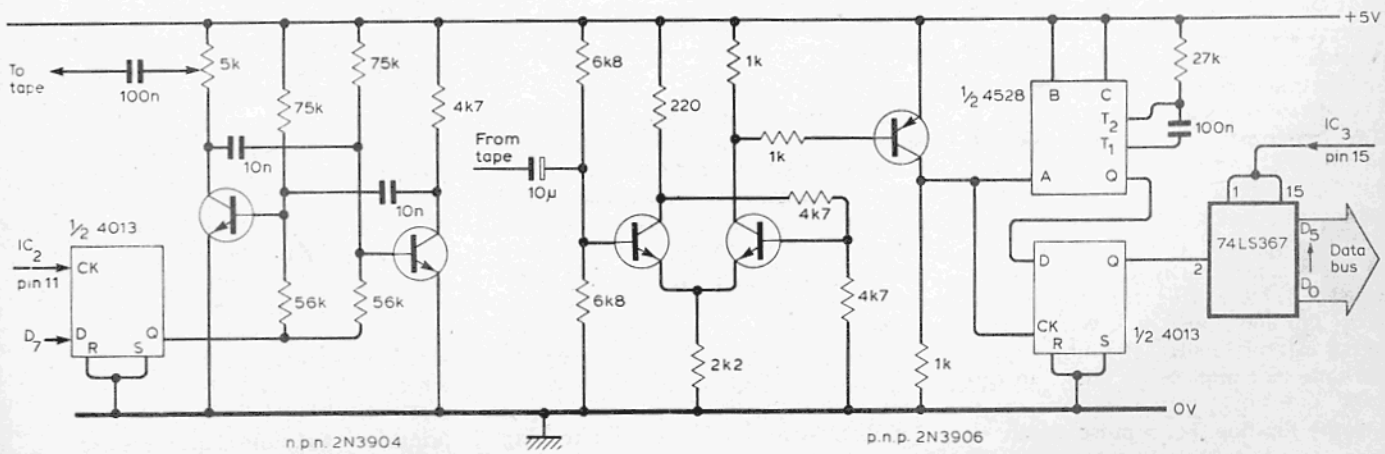
Fig. 12. *Tape interface. The receiver is not susceptible to changes in tape speed because it does not detect a particular frequency, but recognises whether the signal is above or below a certain frequency.*

Each i.c. block in the r/w.m. consists of seven 21L02A4 devices, six of which are used as stores for ASCII character codes. The seventh is for an extension of the v.d.u. to graphical displays and may be omitted. The 2 kilobytes of memory contained in the v.d.u. is mapped at the addresses 8000 to 87FF, but, due to the simple decoding used to address the v.d.u., it may also be "found" at 8800 to 8FFF, 9000 to 97FF etc., up to F800 to FFFF, i.e. 16 blocks in all. This provides a simple method of extending the v.d.u. display so that, after printing out a full screen of results, the next line will automatically start at 8800, i.e. the top of the screen, and so on, which effectively gives over 500 lines of display.

Tv interfacing

The v.d.u. circuit produces approximately 4V of video information and a separate 4V synchronization signal consisting of 4μs and, approximately, 100μs pulses. If a dedicated monitor is not available, perfectly good results can be obtained with a modified 625 line television as follows.

To obtain a high quality display, the video amplifier in the tv set should be ignored, and the v.d.u. signal applied, via a buffer, directly onto the grid of the tube. As the chassis of most sets is connected to one side of the mains, an isolation transformer must be placed between the mains supply and the tv/



computer. Apart from the danger to yourself if this is not done, there is a great risk of destroying several i.cs with one mistake.

A typical interface for a tv set is shown in Fig. 10. If a 30V supply is not available in the set it can be obtained, via a diode and smoothing circuit, from the cathode of the line output stage, or from the computer. The interface should be mounted as close as is possible to the tube base, and the video fed via good quality r.f. coaxial cable from the computer. Capacitor C is selected to compensate for the particular length of coax used, 50pF being a typical value for 1 to 2m of miniature cable.

The best place to inject a sync. signal is where the sync. is taken from the i.f./video section to the timebase. An oscilloscope should be used, with the set operating normally, to identify where the voltage level of the sync. pulses best matches that of the computer. When this has been ascertained it is important to note whether the pulses are positive or negative going, and whether, as is common in valve sets, the entire sync. signal is negative. The first point will determine which sync. output is used, and Fig. 11 shows a simple method of dropping the entire sync. signal below 0V.

Tape interface

It is useful to have a cheap means of storing data and, at present, recording on ordinary cassette tape is the most acceptable method. Blocks of data are recorded onto, or read off tape via the interface shown in Fig. 12.

Data is recorded at 300 baud, with 0s and 1s represented by tones at approximately 1200 and 2400Hz. The Z80 calls the byte to be recorded into register A and sends it out, bit 7 first, along data bus line D_7. The byte is pre fixed by a 0, known as a start bit, and immediately followed by 1½ bits, in duration, of a 1, which is known as a stop bit, see Fig. 13. Thus, the recorded word is 10½ bits long, i.e. 35ms. A time delay is generated by the Z80 (its fastest rate being over 100 Kilobaud) and latches the bits from line D_7 into the D type flip-flop, whose Q output switches a multivibrator to generate the tones.

The receiver consists of a Schmitt trigger and buffer, which produce a 5V pk-to-pk square wave from the tape deck output, followed by a frequency discriminator formed by a monostable and the other half of the D type flip-flop. The square wave at 1200 or 2400Hz is simultaneously used to trigger the monostable, and clock its output into the flip-flop. The pulse width of the monostable has been chosen so that with a triggering rate of 2400Hz, its output is continuously at 1, i.e. a pulse width $>$ 1/2400s. Therefore, the output of the flip-flop is also at 1. With a triggering rate of 1200Hz, the monostable has time to complete its pulse, so the next clocking pulse clocks a 0 into the flip-flop, i.e. a pulse width $<$ 1/1200s. The circuit requires a 2 to 3V pk-to-pk signal from the tape deck.

The firmware starts each recording with several seconds of stop bits before the transmission of data begins, and this allows the tape to be cued before a READ command is given to the computer. The read software operates as shown in Fig. 14.

The bit from the interface is read in through a 6-bit buffer and then masked, i.e. the other bits are blanked off by a Z80 AND instruction, before checking takes place. To give error protection, two checks must indicate that a 0 is being read in before the routine proceeds, and a byte of data is then read in.

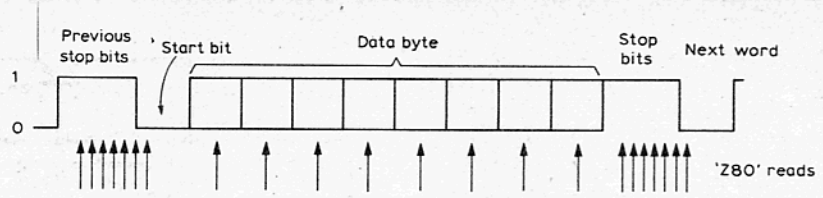


Fig. 13. *Word structure of a software recording.*

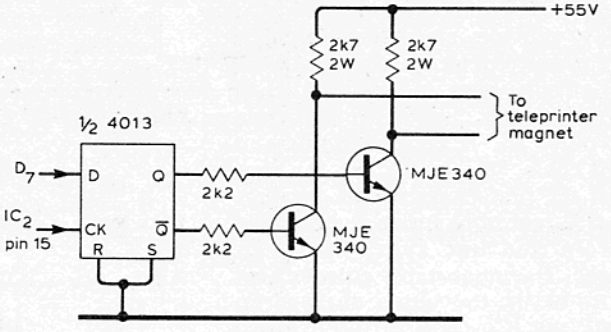


Fig. 15. *Teleprinter interface. This circuit is kept simple because software in the r.o.m. carries out most of the operations.*

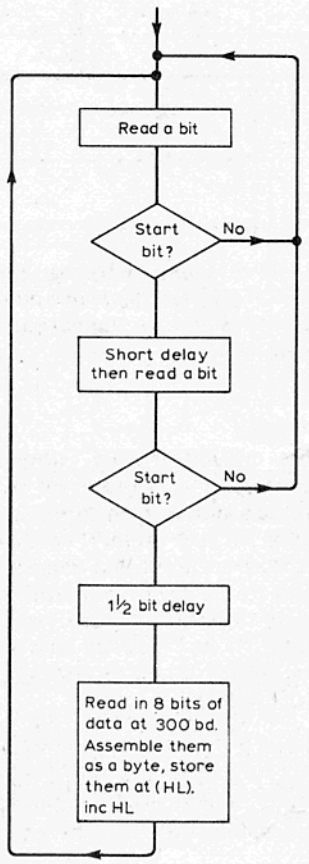


Fig. 14. *Operation of the read software.*

Teleprinter interface

A teleprinter is a very useful addition to any computing system, but, in a low cost design such as this, a new machine would be prohibitively expensive. The supplies of second-hand machines seem to split into two groups; 7/8-bit machines using ASCII coding, and 5-bit machines using modified ASCII or Baudot coding. The advantage of the first type is that they hold the full ASCII set of characters but, they are still reasonably expensive. The 5-bit, modified ASCII machines, such as the Creed 75s, can be purchased for as little as £5, but only have 32 possible codes. Almost 60 different characters can be generated by using two of the code words, 1B and 1F, to switch a mechanical flip-flop, within the teleprinter, between two sets of characters, letters or figures and punctuation. The two shift characters, line feed, carriage return, blank and space remain common to both shifts.

This type of machine requires a serial input at 75 baud which means that, with a 7½-bit word, it will print 10 characters per second. Coding for the letters is identical to the lower 5 bits of ASCII code, but the figures, although similar, require translating from the 6-bit subset of ASCII used in the computer, to the 5-bit code for the teleprinter. The formation of words comprising a start bit, five data bits and two stop bits, the interspersing of figure and letter shifts where necessary, the storage of a byte which mirrors the state of the mechanical shift flip-flop in the teleprinter so that shift characters are only

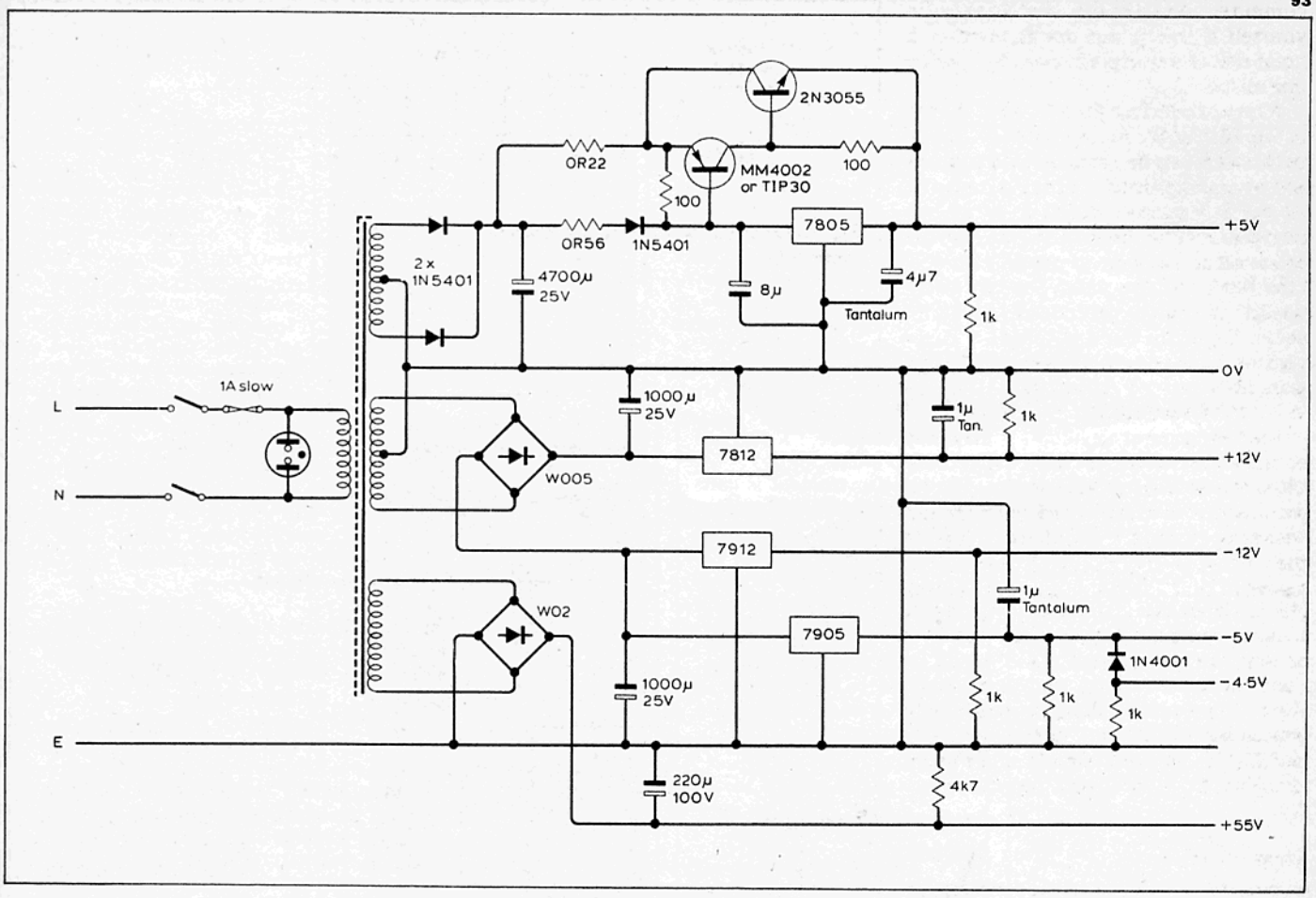


Fig. 16. *Power supply. A 1A regulator in parallel with a general purpose power transistor gives a regulated output of up to 3.5A.*

sent when necessary, and the time delays required to slow the computer down to 75 baud, are all accomplished by software stored in part of the monitor r.o.m. The hardware involved in interfacing the teleprinter, Fig.15, is therefore very simple.

Power supplies

The power supply provides stabilized outputs of +5V at 3.5A, −5V and ±12V at 1A, and an unstabilized output of approximately + 55V at 100mA. The +5V supply in Fig. 16 is the only unusual part of the circuit as it uses a 1A regulator i.c. with a pseudo p-n-p pass transistor instead of a more expensive 3A regulator. The circuit operates by dividing the current passing through the regulator and the transistor in the ratio of the two series resistors. In this case, 56/22 times as much current passes through the 2N3055, which gives a 3.5A regulated output for 1A through the 7805. It is important that the regulator, transistors, and the diode which mirrors the voltage drop across the base-emitter junction of the p-n-p transistor are in good thermal contact.

The −4.4V supply is for the MM57109 which is specified to operate from a maximum overall supply of 9.5V. The +55V supply is for the teleprinter magnet. Although the Creed magnets, in common with others, are designed to operate with a current of 20mA, and have a resistance of 200Ω, switching 4V into the coil is not satisfactory due to the inductance in the magnet's coil. Therefore, current driving, rather than voltage supplying, is required to produce a quick action from the magnets, and a high voltage supply fed through 2.7kΩ resistors is used. If a teleprinter is not going to be used, it is still worth including this supply as it may be needed for the tv interface, and will be required for the r.o.m. programmer to be described later.

The transformer used in the prototype was an RS Components 50VA d.i.y. type 207-554 with windings to give open-circuit voltages of 9.5-0-9.5V for the +5V supply, 13V for the −5V and ±12V supply, and 40V for the teleprinter supply, the last mentioned being wound with 36 s.w.g. wire and the other two with 22 s.w.g. wire.

No filtering has been included at the mains input as the processor is relatively insensitive to interference from the mains cable. The computer has been used to receive radioteleprinter messages via a communications receiver with an interface, and tests showed that negligible interference leaves the computer by the mains cable.

To be continued

A kit of parts for constructing a computer on this design is available from Powertran Computers, Portway Industrial Estate, Andover, Hants SP10 3NN (tel: Andover (0264) 64455).

The author

John Adams read for a B.Sc. in electronic engineering and for an M.Sc. in materials science, at the University College of North Wales, before becoming a teacher. His involvement in electronics is, therefore, primarily as an amateur, and the design for this computer started 18 months ago as an exercise to gain familiarity with microprocessors. John operates the amateur radio station G3VZF, and in his spare time claims to be a very amateur musician.